LOW AREA LINEAR TIME-DRIVER CIRCUIT

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TECHNICAL FIELD

The present invention provides a low space consuming linear time-driver circuit that is based upon the small capacitor charge of the merged region of a 5V tolerant cascoded NMOS device, a single gate device and a zener diode.

DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit schematic illustrating a time-driver circuit in accordance with the concepts of the present invention that utilizes a cascoded NMOS design.

Fig. 1B is a partial cross-section drawing of an emodiment of the Fig. 1A circuit taken along the cascoded NMOS device structure of Fig. 1A.

Figs. 1C and 1D are graphs illustrating merged region node voltage over time for various capacitor values for the Fig. 1A/1B circuit.

Figs. 2A and 2B are graphs illustrating the calculated transient characteristic for merged region node voltage as a function of the capacitor, the gate resistive divider ratio and the V_{DD} level for the Fig. 1 circuit.

Fig. 3 is a circuit schematic illustrating a time-driver circuit in accordance with the concepts of the present invention that utilizes a non-cascoded NMOS design.

Fig. 3B is a partial cross section drawing of an embodiment of an NMOS device in the Fig. 3 circuit.

Fig. 4 is a graph illustrating the calculated transient characteristic for the merged region node voltage as a function of the capacitor, the gate resistive divider ratio and the V_{DD} level for the Fig. 3 circuit.

DESCRIPTION OF THE INVENTION

Time-driver circuits are one of the important elements for the active clamps used in electrostatic discharge (ESD) protection circuits. Because simple, but space-consuming RC-timers are typically used in these ESD application, the drivers are typically implemented as corner cells in the overall circuit layout. As a result, the timer time domain is limited by 6-8 usec.

Fig. 1A shows a time-driver circuit 100 in accordance with the concepts of the present invention that utilizes a cascoded NMOS design. Fig. 1B shows a cross-section of an embodiment of the Fig. 1A time-driver circuit taken along the cascoded NMOS structure of the Fig. 1A circuit 100.

The Fig. 1 circuit 100 includes cascoded NMOS devices 102 and 104 connected between a positive voltage supply V_{DD} and a negative voltage supply V_{SS}. The gate of the lower NMOS device 104 is connected to the negative voltage supply V_{SS} by a resistor R_G. The gate of the upper NMOS transistor 102 is connected to the common node of a resistive divider 108 that includes resistor R_{D1} and resistor RD2. The merged (common) node 110 of the cascoded NMOS devices 102 and 104 provides a capacitive charge C_T that is disposed between the cascoded structure common node 110 and the positive voltage supply V_{DD}.

Evaluation of the circuit 100 shown in Fig. 1B has demonstrated that a linear voltage dependence is produced in a wide range of parameters under extremely small component values. The cascoded NMOS device utilized for the Fig. 1B test circuit was taken at w=10 microns. The millisecond range is achieved for a capacitor value C_T of about 100f only.

The output node voltage V(t) of the circuit is supposed to be loaded on the circuit starting with the low equivalent capacitance input realized by minimum dimension devices.

The operational principle of the circuit is as follows. Under initial conditions, V_{DD} = 0, the capacitor C_T is discharged and the potential of the cascoded structure common node 110 is equal to $V_{DD} = 0$. The gate potential of the lower NMOS device 104 is also zero. The gate potential of the upper NMOS device 104 is defined by the ratio R_{D1}/R_{D2} of the resistive divider 108. After the positive supply V_{DD} is applied and a fast current through the parasitic capacitance C_T of the device, the potential of the merged cascoded structure common node 110 starts to change due to the charge of the capacitor C_T. The gate potential of the lower

NMOS device 104 remains zero. The gate potential of the upper NMOS device 102 is defined by the ration R_{D1}/R_{D2} of the resistive divider 108 and is lower than the potential of the cascoded structure common node 110. Thus, both NMOS devices 1-2 and 104 are in the off state. The capacitor C_T continues to charge by the leakage current through the upper NMOS device 102 until equilibrium is defined by the gate potentials.

Figs. 1C and 1D are graphs showing voltages of the merged cascoded structure common node 110 over time for various capacitor values C_T for the Fig. 1A/1B circuit.

Figs. 2A and 2B are graphs that illustrate the calculated transient characteristics for the merged region node voltage as a function of the capacitor C_T, the gate resistive divider ratio R_{D1}/RD2 and the V_{DD} level for the Fig. 1A/1B circuit.

Those skilled in the art will appreciate that similar principles can be realized for a 3.3V or lower tolerant voltage based on a non-cascoded NMOS design, as shown in Fig. 3A. Fig. 3B shows a cross-section of an embodiment of an NMOS device 202 in the Fig. 3A circuit 200.

The Fig. 3A circuit 200 includes an NMOS device 202 that is connected between a positive supply V_{DD} and a negative supply V_{SS}. The gate of the NMOS device 202 is connected to the common node 204 of a resistive divider 206 that includes a resistor R_{D3} that is connected between the positive supply C_{DD} and the resistive divider common node 204 and a resistor R_{D4} that connected between the resistive divider common node 204 and the negative supply V_{SS}. As in the case of the cascoded NMOS design discussed above in conjunction with Figs. 1A/1B, a capacitor C_T is connected between the output V(t) of the NMOS device 202 and the positive supply V_{DD}.

Fig. 4 is a graph that shows the calculated transient characteristic for the merged region node voltage as a function of the capacitor C_T, the resistive divider ratio R_{D3}/R_{D4} and the V_{DD} level for the Fig. 3A non-cascoded circuit 200.

It should be understood that various alternatives to the embodiments of the invention described herein may be employed in practicing the invention. It is intended that the following claims define the scope of the invention and structures and methods within the scope of these claims and their equivalence be covered thereby.

5